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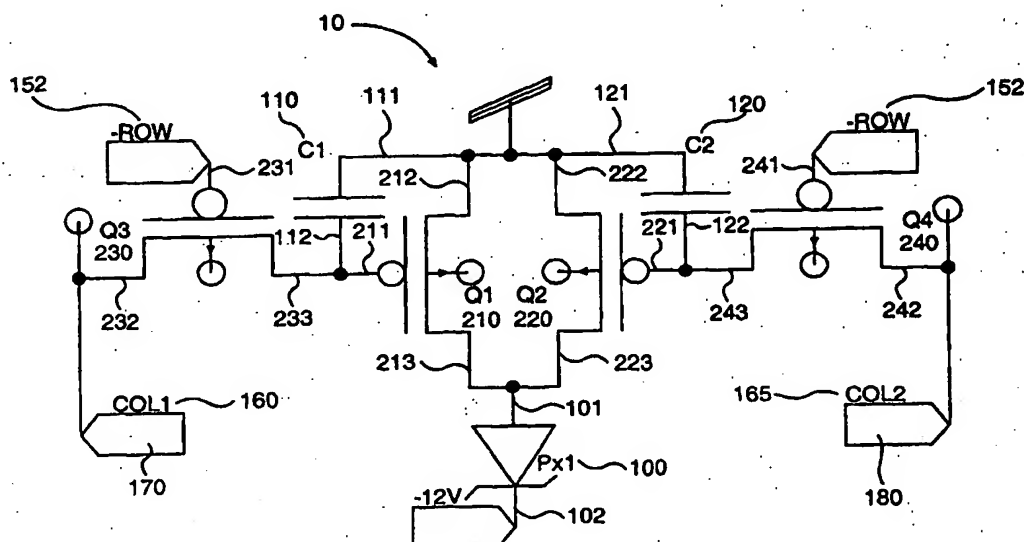
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(54) Title: **IMPROVED PIXEL DRIVER FOR ACCURATE AND FINER GRAY SCALE RESOLUTION**



(57) Abstract

A pixel driver circuit for a flat panel display is disclosed. The circuit design employs at least one storage capacitor (110) for each pixel (100) and uses digital-to-analog converters (170, 180) to subdivide the digital pixel brightness input data and provide enhanced gray scale resolution. The subdivided data are converted to analog input data and are controlled using constant amplitude pulses. The relatively large voltage output steps of the present invention reduce the error in the pixel brightness from line voltage drops and coupled noise.

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## **IMPROVED PIXEL DRIVER FOR ACCURATE AND FINER GRAY SCALE RESOLUTION**

### **Cross Reference to Related Applications**

This application relates to and claims priority on United States Provisional Application Serial No. 60/080,596, filed April 3, 1998 and entitled "Two Storage Capacitor Pixel Driver for Improved Finer Gray Scale Resolution."

### **Field of the Invention**

The present invention relates to flat panel display devices. In particular, the present invention relates to a circuit design that significantly enhances the gray scale resolution of a pixel in a display device. Specifically, the circuit design employs at least one storage capacitor for each pixel and uses digital-to-analog converters to subdivide the digital pixel brightness data.

### **Background of the Invention**

Flat panel image display devices are well-known in the art. Examples of such display devices include field emission displays (FEDs), liquid crystal displays (LCDs), plasma displays and electroluminescent displays. A wide variety of software applications are used with such image display devices. Software applications such as word processing, spreadsheets and other applications rely heavily on gray shades to provide high quality graphics and video. A major factor in the overall quality of the displayed picture, whether color or monochrome, is gray level accuracy in the individual pixels.

The prior art includes several methods of controlling the drive signals that produce gray levels in image display devices. One method, known as pulse width modulation, uses a digital video word to encode the intensity of an image that is to be displayed by the image display device during a particular display time. Another method for controlling the drive signals that produce gray levels is known as amplitude modulation. This method varies the voltage value applied to each pixel to control the intensity. Known devices using amplitude modulation have been susceptible to noise because of the low drive voltage increments used, which results in a loss of display quality.

U.S. Patent No. 5,477,110 to Smith et al. is directed to a pulse width modulation method of controlling a field emission device. In connection with a cold cathode emitter device, Smith et al. disclose subdividing the input 8-bit word (i.e., picture brightness) into two four (4)-bit nibbles of high nibble data and low nibble data. A first current source is turned on based on the high nibble data. A second current source is turned on based on the low nibble data. The two current sources provide pulse width modulation of the pixel current with a high degree of accuracy.

In contrast, the present invention utilizes the two nibbles to control the voltages developed across two capacitors which directly control the total pixel current. This method uses less circuitry, which consumes less power and is more compact. These are important features for portable, battery-operated systems. Additionally, the present invention is more suited for high resolution applications where the pixel count per line is high and the time available per pixel is too small for pulse width modulation.

U.S. Patent No. 4,030,090 to Endriz is also directed to a pulse width modulation display device. Endriz discloses a flat cathode luminescent image display device employing a modulation mask which uses digital control circuitry. The devices use an electron multiplier to intensify the electron beam. Accelerating and gating electrodes with built-in capacitance are also included to control the flow of electrons to the final target, the light-emitting anode layers. The device is enclosed in an evacuated glass envelope. The panel thickness is 2.5 cm, in order to include the critical components of the pixel cell, including a photoemissive barium cathode, optical feedback to sustain electron emissions, the electron multiplier, high energy electron filters, accelerators, and focusing structures. This design requires vacuum sealed units with sufficient mechanical supports to avoid implosion.

In contrast to U.S. Patent No. 4,030,090, the present invention design uses only hermetic sealing without a vacuum and does not require the complex electron gun or its associated complex control elements. The simplicity of the present invention permits the pixel size to be reduced to approximately 0.01 mm width by 0.01 mm height. Such orders of magnitude differences in pixel size render the techniques used in U.S. Patent No. 4,030,090 inapplicable to the present invention. In addition, the present invention uses a low voltage (+12 V), low power (battery operated) system rather than the high voltage (+50), high power system disclosed in U.S. Patent No. 4,030,090.

The technique disclosed in U.S. Patent No. 4,030,090 uses standard pulse width modulation and adjusts the amplitude of the last two pulses to accomplish better gray scale resolution. In contrast, the present invention uses constant amplitude pulses to control the device drive signals, but instead of lining up the pulses side-by-side as in pulse width modulation, the pulses are effectively piled on top of each other, as in amplitude modulation, to accomplish a similar goal.

The design of the present invention is developed for a high density, low power, lightweight, and compact product with no associated memory, whereas U.S. Patent No. 4,030,090 is not capable of meeting these requirements. The pixel size of the design disclosed in U.S. Patent No. 4,030,090 is approximately 14,000 times larger than the pixel size of the present invention. The known art comprises other patents employing techniques for modulating the electron beams of the display to enhance brightness. For example, U.S. Patent No. 4,077,054 to Endriz is directed to a method for enhancing the accuracy of pixel brightness. The charge build-up on the screen of a display panel is proportional to the brightness of the light output from the pixel. An assembly is provided for generating a voltage that is proportional to the instantaneous charge on the screen and the pixel brightness. The voltage is compared with the video input data and the current feed to the screen is automatically cut off when the correct level is reached. This approach is unrelated to that of the present invention.

Another example of display modulation is disclosed in U.S. Patent No. 4,051,468 to Rajchman. This design is identical to that in U.S. Patent No. 4,077,054, namely the comparison of the electrical charge striking the screen's surface with the image brightness signal. It is also unrelated to the present invention.

U.S. Patent No. 5,404,074 to Watanabe et al. discloses a cold cathode emitter device. A storage capacitor is used with each pixel to stretch the duration of the pixel current to the full frame period to get enhanced brightness at lower anode voltages. This approach is unrelated to that of the present invention.

Another example of a cold cathode emitter device is disclosed in U.S. Patent No. 5,283,500 to Kochanski. This design uses series capacitors to improve the uniformity of illumination and provide protection against internal short circuits between the cathode and the grid. This design is unrelated to the present invention.

U.S. Patent No. 5,572,231 to Kobori discloses blanking pulses applied to gate electrodes in a drive device for a field emission display. These blanking pulses are intended to increase the switching speed and suppress spurious emissions normally present at the beginning of light emission. The design is unrelated to the present invention.

5 U.S. Patent No. 5,642,017 to Hush is directed to a pixel control circuit for flat panel field emission matrix-addressable array display. This circuit employs a single transistor per pixel and includes individual series resistors. Pixel brightness is controlled by a current-limiting resistor. The circuit is unrelated to the present invention.

10 U.S. Patent No. 5,617,111 to Saitoh discloses a circuit for driving a liquid crystal device. This circuit subdivides the incoming digital data into the most significant half and the least significant half. The decoded output voltage of the most significant half is applied to one end of the capacitor. The decoded output voltage of the least significant half is applied to the other end of the capacitor. An output amplifier is used to output the sum of the two voltages to drive the pixel. Better gray scale reproduction is achieved with a reduced number of external voltage  
15 supplies. It is common to use a single capacitor in connection with a pixel cell.

In contrast, the present invention may employ two separate capacitors. The arrangement of the present invention provides better noise immunity with improved accuracy of the gray scale reproduction with high density, low power and high speed applications.

20 U.S. Patent No. 5,566,010 to Ishii et al. discloses a liquid crystal display that is capable of providing a high precision and bright display. The driving circuit for the display includes a pair of capacitors. These storage capacitors mask the delay that arises between the application of a polarizing voltage to the liquid crystal layer and the corresponding liquid crystal molecules. While one pixel is lit with the data previously stored in the first capacitor, the second pixel is fed the data stored in the second capacitor, preparing that second pixel for illumination. This use  
25 of two storage capacitors in U.S. Patent No. 5,566,010 is unrelated to the present invention.

In the present invention, Applicants disclose a design using a variation of amplitude modulation that is less susceptible to excess noise and provides significantly enhanced gray scale resolution. The use of digital-to-analog converters permits each voltage output step to be relatively large, which reduces the error in pixel brightness. In addition, the use of one or more  
30 capacitors in the circuit enhances the accuracy of the gray scale through greater noise immunity.

### Objects of the Invention

It is therefore an object of the present invention to provide a display device driver system that provides sharper pictures in pixel arrays.

It is another object of the present invention to provide a display device driver system that improves the accuracy of gray scale reproduction.

It is yet another object of the present invention to provide a display device driver system that provides sharper pictures in pixel arrays through improved accuracy of the gray scale reproduction in high density, low power, and high speed applications.

It is still another object of the present invention to provide a display device driver system that enhances the gray scale resolution in lightweight, compact, and portable product applications.

It is a further object of the present invention to provide simple circuitry to produce improved gray scale resolution in a display device.

It is another object of the present invention to enhance significantly the accuracy with which the digital gray level input data are translated into actual pixel brightness.

It is still another object of the present invention to provide a driver system with large voltage output steps in order to reduce the error introduced in the pixel brightness from line voltage drops or coupled noise.

It is another object of the present invention to maintain the accuracy of the gray scales in a practical manufacturing environment.

It is another object of the present invention to reduce pixel size in a display device.

It is another object of the present invention to provide a display device driver system with improved noise immunity.

Additional objects and advantages of the invention are set forth, in part, in the description which follows and, in part, will be apparent to one of ordinary skill in the art from the description and/or from the practice of the invention.

### Brief Summary of the Invention

In response to this challenge, Applicant has developed an innovative, economical, simple pixel driver circuit for a video display device having a plurality of pixels arranged in a matrix. The pixel driver circuit may use constant amplitude pulses to control the device drive signals,

thereby providing a high density, low power, lightweight, and compact product with no associated memory. The driver circuit may comprise means for supplying digital pixel brightness input data; means for subdividing the digital input data, connected to the supplying means; means for converting the subdivided digital input data to analog input data, connected to the subdividing means; means for applying the analog input data to the driver circuit, connected to the converting means; at least one capacitor connected to the applying means; and means for feeding the analog input data to one of the plurality of pixels, connected to the applying means and to the at least one capacitor.

The applying means may comprise at least one p-type field effect transistor. The means for feeding the analog input data to one of the plurality of pixels may comprise at least one p-type field effect transistor. The digital input data may comprise 8 bits of data. The subdivided digital input data may comprise a first half-byte of four higher order bits and a second half-byte of four lower order bits. The converting means may comprise a first digital-to-analog converter for the four higher order bits and a second digital-to-analog converter for the four lower order bits.

The first digital-to-analog converter may convert the four higher order bits of digital input data into analog data of a first plurality of current values. The first plurality of current values may comprise 16 discrete steps of 16nA each, to cover a range of 0 to 256nA.

The second digital-to-analog converter may convert the four lower order bits of digital input data into analog data of a second plurality of current values. The second plurality of current values may comprise 16 discrete steps of 1nA each, to cover a range of 0 to 16nA.

In another embodiment, the applying means may comprise at least one p-type field effect transistor and at least one n-type field effect transistor.

In another embodiment, the pixel driver circuit for a video display device may have a plurality of pixels arranged in a matrix, may use constant amplitude pulses to control the device drive signals, and may comprise means for supplying digital pixel brightness input data; means for converting the digital input data to analog input data, connected to the supplying means; means for applying the analog input data to the driver circuit, connected to the converting means; at least one capacitor connected to the applying means; and means for feeding the analog input data to one of the plurality of pixels, connected to the applying means and to the at least one capacitor. The applying means may comprise at least one p-type field effect transistor. Further,



the means for feeding the analog input data to one of the plurality of pixels may comprise at least one n-type field effect transistor; and the digital input data may comprise 8 bits of data. The embodiment may further comprise a strobe column line. Alternatively, a ramp control line may be used.

5           Applicant further discloses a method of driving a pixel circuit in a video display device having a plurality of pixels arranged in a matrix and using constant amplitude pulses to control the device drive signals, comprising the steps of receiving a byte of digital pixel brightness input data; dividing the digital byte into a first half-byte of four higher order bits and a second half-byte of four lower order bits; converting the first half-byte into a first analog input signal;  
10           converting the second half-byte into a second analog input signal; applying the first analog input signal and the second analog input signal to the driver circuit; storing a charge on at least one capacitor in response to the analog input signals; feeding the first analog input signal and the second analog input signal to one of the plurality of pixels; and controlling the voltages developed across the at least one capacitor to directly control the total current fed to one of the  
15           plurality of pixels.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only, and are not restrictive of the invention as claimed. The accompanying drawings, which are incorporated herein by reference, and which constitute a part of this specification, illustrate certain embodiments of the invention, and  
20           together with the detailed description serve to explain the principles of the present invention.

### Brief Description of the Drawings

The invention will now be described in conjunction with the following drawings in which like reference numerals designate like elements and wherein:

25           Fig. 1 depicts a schematic diagram of a pixel driver circuit with two storage capacitors according to a preferred embodiment of the present invention;

Fig. 2 depicts a schematic diagram of a digital-to-analog converter for the four higher order bits according to the present invention;

Fig. 3 depicts a schematic diagram of a digital-to-analog converter for the four lower  
30           order bits according to the present invention;

Fig. 4 depicts a schematic diagram of a pixel driver circuit with two storage capacitors according to another embodiment of the present invention;

Fig. 5 depicts a schematic diagram of a pixel driver circuit with four capacitors according to another embodiment of the present invention;

5 Fig. 6 depicts a schematic diagram of a common cathode pixel cell driver with one capacitor for a high voltage process according to another embodiment of the present invention; and

Fig. 7 depicts a schematic diagram of a common cathode pixel cell driver with one capacitor and a ramp control line according to another embodiment of the present invention.

### Detailed Description of Preferred Embodiments

Reference will now be made in detail to preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. A first embodiment of a pixel driver circuit for improved gray scale resolution for video displays according to the present invention is shown in Fig. 1 as 10. Referring to Fig. 1, two capacitors C1 110 and C2 120 are provided. First end 111 of capacitor C1 110 is connected to source 212 of first transistor Q1 210 and tied to positive voltage supply Vdd. First end 121 of capacitor C2 120 is connected to source 222 of second transistor Q2 220 and tied to positive voltage supply Vdd. Second end 112 of capacitor C1 110 is connected to gate 211 of first transistor Q1 210 and tied to drain 233 of third transistor Q3 230. Second end 122 of capacitor C2 120 is connected to gate 221 of second transistor Q2 220 and tied to drain 243 of fourth transistor Q4 240. Gate 231 of third transistor Q3 230 and gate 241 of fourth transistor Q4 240 are connected to complement to row line -ROW 152. Source 232 of third transistor Q3 230 is connected to first column line COL1 160. Source 242 of fourth transistor Q4 240 is connected to second column line COL2 165. Drain 213 of first transistor Q1 210 and drain 223 of second transistor Q2 220 are tied together and connected to anode 101 of pixel Px1 100. Cathode 102 of pixel Px1 100 is connected to a negative voltage (-12V) supply. Transistors Q1 210, Q2 220, Q3 230, and Q4 240 are preferably p-type field effect transistors (P-FETs).

As embodied herein, the 8-bit digital pixel brightness input data are subdivided into two "half-bytes." Each half-byte contains 4-bits. The half-byte containing the four higher order bits

is designated as the upper half byte ("UHB"). The half-byte containing the lower four bits is referred to as the lower half-byte ("LHB").

Referring now to Fig. 2, a digital-to-analog converter for the four higher order bits or upper half byte (UHB) is shown as 170. D/A converter 170 comprises a P-FET transistor connected to positive voltage supply Vdd, four resistors of varying values R, R/2, R/4 and R/8, and four digital input transistors that receive the UHB digital input data. D/A converter 170 is incorporated in first column line COL1 160, and is known in the art. D/A converter 170 for the UHB operates as follows: using the resistor values as shown, the current drawn by the P-FET transistor covers the range 0 through 15I in steps of I. The actual value of the current at any time is controlled by the four digital inputs IN4 through IN7. The voltage at the output node at first column line COL1 160 is therefore such that when applied to gate 211 of P-FET device Q1 210 in the pixel of Fig. 1, the current output of Q1 210 will correspond to the digital input data IN4 through IN7.

Referring now to Fig. 3, a digital-to-analog converter for the four lower order bits or lower half byte (LHB) is shown as 180. D/A converter 180 comprises a P-FET transistor connected to positive voltage supply Vdd, four resistors of varying values 16R, 8R, 4R, and 2R, and four digital input transistors that received the LHB digital input data. D/A converter 180 is incorporated in second column line COL2 165, and is known in the art. D/A converter 180 for the LHB operates as follows: using the resistor values as shown, the current drawn by the P-FET transistor covers the range 0 through  $(15/16) \times I$  in steps of  $(1/16) \times I$ . The actual value of the current at any time is controlled by the four digital inputs IN0 through IN3. The voltage at the output node of second column line COL2 165 is therefore such that when applied to gate 221 of P-FET device Q2 220 in the pixel of Fig. 1, the current output of Q2 220 will correspond to the digital input data IN0 through IN3.

D/A converter 170 is incorporated into first column line COL1 160 and D/A converter 180 is incorporated into second column line 165

The circuit of Fig. 1 operates as follows: input current is drawn through D/A converters 170 and 180, which convert the digital input data to analog input voltages as described above. The analog input voltage from D/A converter 170 is fed to COL1 160, while the analog input voltage from D/A converter 180 is fed to COL2 165. The voltage from COL1 160 is applied to gate 211 of transistor Q1 210 and capacitor C1 110. The voltage from COL2 165 is applied to

gate 221 of transistor Q2 220 and capacitor C2 120. The analog input voltages are fed to capacitors C1 110 and C2 120 by first column line COL1 160 and second column line COL2 165 through the row selected P-FETs Q3 230 and Q4 240. The output currents of transistor Q1 210 and transistor Q2 220 are fed to pixel diode Px1 100. Capacitors C1 110 and C2 120 may be  
5 charged or discharged by switching on transistors Q3 230 and Q4 240 by bringing down -ROW line 152 and applying appropriate analog input voltages to first column line COL1 160 and second column line COL2 165. In this embodiment,  $W/L = 4/1$  for transistor Q1 210 and  $W/L = 1/4$  for transistor Q2 220. In the linear operating range, the current output of transistor Q1 210 for a given input voltage is 16 times that of transistor Q2 220. Accordingly, the  
10 transconductance of Q1 210 is 16 times greater than that of Q2 220.

In this embodiment, the total pixel current in pixel Px1 100 is the sum of the currents supplied by Q1 210 and Q2 220 and will thus correspond to the digital input data contained in the 8-bit digital input lines IN0 through IN7, that is, a total of 256 gray levels. There are only  
15 16 analog voltage output levels in the two D/A converters 170 and 180 so that each voltage output step is relatively very large as compared with the 256 output steps of a conventional single D/A converter used in one-capacitor pixel cells. The large steps of the present invention significantly reduce the overall error introduced in the pixel brightness due to line voltage drops, coupled noise, etc. which are always present in actual circuits. The input voltage range of first transistor Q1 210 is sliced into 16 discrete steps of 16nA input current each, to cover a range of  
20 0 to 256nA. The input voltage range of second transistor Q2 220 is also sliced into 16 discrete steps of 1nA each to cover the range of 0 to 16nA. The higher four bits of the input digital data generate the desired voltage level for the current to Q1 210 while the lower four bits of the input data provide the "fine tuning" to get to the correct gray level. Since the input dynamic range of 4.5 volts is sliced into 16 pieces by the D/A converters, the errors associated with very fine  
25 slicing (256 slices) used in known pixel cell designs are significantly reduced.

Referring now to Fig. 4, another alternate embodiment is shown as 20. In this alternate embodiment, two additional devices Q5 250 and Q6 260 are added to cancel out the effects of the gate-to-drain capacitors of Q3 230 upon the charges stored in first capacitor C1 110 and second capacitor C2 120. First end 111 of capacitor C1 110 is connected to source 212 of first transistor Q1 110 and tied to positive voltage supply Vdd. First end 121 of capacitor C2 120 is  
30 connected to source 222 of second transistor Q2 220 and tied to positive voltage supply Vdd.

Second end 112 of capacitor C1 110 is connected to gate 211 of first transistor Q1 210 and tied to drain 223 of third transistor Q3 230 and to drain 253 of fifth transistor 250. Second end 122 of capacitor C2 120 is connected to gate 221 of second transistor Q2 220 and tied to drain 243 of fourth transistor Q4 240 and to drain 263 of sixth transistor Q6 260. Gate 231 of third transistor Q3 230 and gate 241 of fourth transistor Q4 240 are connected to complement to row line -ROW 152. Source 232 of third transistor Q3 230 and source 252 of fifth transistor Q5 250 are tied together and connected to first column line COL1 160. Source 242 of fourth transistor Q4 240 and source 262 of sixth transistor Q6 260 are tied together and connected to second column line COL2 165. Drain 213 of first transistor Q1 210 and drain 223 of second transistor Q2 220 are tied together and connected to anode 101 of pixel Px1 100. Cathode 102 of pixel Px1 100 is connected to negative voltage.

Gates 251 and 261 of fifth transistor Q5 250 and sixth transistor Q6 260 are connected to external signal ROW 150, which is the complement of the -ROW 152 signal used with third transistor Q3 230 and fourth transistor Q4 240. Devices Q5 250 and Q6 260 are preferably n-type field effect transistors (N-FETs).

The alternative embodiment 20 shown in Fig. 4 operates as follows: When -ROW 152 goes up to turn off transistor Q3 230 and transistor Q4 240, ROW 150 goes down to turn off transistor Q5 250 and transistor Q6 260 and vice versa. The input data get additional parallel paths to first capacitor C1 110 and second capacitor C2 120, and the circuit remains unchanged from circuit 20 shown in Fig. 4 except that the additional unwanted charges supplied to capacitors C1 110 and C2 120 by the gate-drain capacitors of third transistor Q3 230 and fourth transistor Q4 240 are neutralized by equal but opposite charges supplied by the gate-to-drain capacitors of fifth transistor Q5 250 and sixth transistor Q6 260. To net it out, the effects of the gate-drain capacitors of devices Q3 230 and Q4 240 may be neutralized by adding the two extra complimentary devices Q5 250 and Q6 260, along with an extra complimentary row drive.

Referring now to Fig. 5, another alternate embodiment of the present invention is shown as 30. In this alternate embodiment, pixel driver circuit 30 is provided with third capacitor C3 130 and fourth capacitor C4 140, replacing transistors Q5 250 and Q6 260 shown in embodiment 20 of Fig. 4. First end 131 of capacitor C3 130 is connected to row line ROW 150. Second end 132 of capacitor C3 130 is connected to gate 211 of first transistor Q1 210 and tied to drain 223 of third transistor Q3 230 and to second end 112 of capacitor C1 110. First end 141

of capacitor C4 140 is also connected to row line ROW 150. Second end 142 of capacitor C4 140 is connected to gate 221 of second transistor Q2 220 and tied to drain 243 of fourth transistor Q4 240 and to second end 122 of capacitor C2 120.

Capacitors C3 130 and C4 140 are equivalent to gate-to-drain capacitors of Q3 230 and Q4 240, respectively. Since Q3 230 and Q4 240 are very small, they may be implemented as simple overlap capacitors between two conducting layers.

Referring now to Fig. 6, an alternate embodiment of the present invention is shown as 40. In this embodiment, a common cathode pixel cell for a high voltage process is provided. Pixel cell 40 is provided with a single capacitor C1 110 and a single D/A converter 185 that converts all 8-bits of digital pixel brightness input data into analog voltage. D/A converter 185 is incorporated into column line DATA 169. First end 111 of capacitor 110 is connected to positive voltage supply Vdd and to source 242 of fourth transistor Q4 240. Second end 112 of capacitor 110 is connected to gate 241 of fourth transistor Q4 240 and drain 233 of third transistor Q3 230. Gate 211 of first transistor Q1 210, gate 221 of second transistor Q2 220, and gate 251 of fifth transistor Q5 250 are tied to row line -ROW 152. Gate 231 of third transistor Q3 230 is tied to drain 213 of first transistor Q1 210. Source 212 of first transistor Q1 210 is tied to column strobe line -STR 168. Source 222 of second transistor Q2 220 is tied to column line DATA 169. Source 232 of third transistor Q3 230 is connected to drain 223 of second transistor Q2 220. Drain 243 of fourth transistor Q4 240 is connected to drain 253 of fifth transistor Q5 250. Source 252 of fifth transistor Q5 250 is connected to anode 101 of pixel Px1 100. Cathode 102 of pixel Px1 100 is connected to negative voltage. Third transistor Q3 230 and fourth transistor Q4 240 are preferably P-FETs. Fifth transistor Q5 250 is preferably an N-FET.

The circuit of Fig. 6 operates as follows: digital pixel brightness input data are converted to analog voltage by D/A converter 185. When the input analog voltage on column line DATA 169 is valid, row and column are selected by bringing down -ROW 152 and column -STR 168 lines to turn on transistors Q1 210, Q2 220 and Q3 230. The analog voltage on DATA line 169 passes through Q2 220 and Q3 230 to charge up storage capacitor C1 110 connected to gate 241 of output device Q4 240. Once capacitor C1 110 is charged up, -STR line 168 is brought up (+5V) to switch off transistor Q3 230 via transistor Q1 210. This operation does not affect the voltage stored on capacitor C1 110 except for the switching transient passed on through the gate-drain capacitance of Q3 230.

Next, the row line is deselected by bringing up -Row line 152 to +5volts, thereby turning off transistors Q1 210 and Q2 220; transistor Q3 230 is already off. Also, since gate 250 of fifth transistor Q5 250 is tied to the row line -ROW 152, device Q5 250 turns on at this time and the output current of Q4 240 is supplied to pixel Px1 100. Cathode 102 of pixel Px1 100 is tied to -12volts. The pixel current depends upon the voltage stored on the capacitor and continues to flow through pixel Px1 100 until row line -ROW 152 is selected again during the next frame period. Then the cycle is repeated. The design of the present invention is simple and provides nearly a 100% duty cycle so that maximum brightness level can be achieved with relatively very low pixel current. The result is improved accuracy of gray scale resolution.

Referring now to Fig. 7, another alternate embodiment of the present invention is shown as 50. In this alternate embodiment, pixel driver circuit 50 is a modification of circuit 40 shown in Fig. 6. As embodied herein, source 242 of fourth transistor Q4 240 is disconnected from the +5V (Vdd) supply and is tied to external node RAMP 190. As in circuit 40 described above, pixel cell 50 is provided with single capacitor C1 110 and a single D/A converter 185 that converts all 8-bits of digital pixel brightness input data into analog voltage. D/A converter 185 is incorporated into column line DATA 169. First end 111 of capacitor 110 is connected to positive voltage supply Vdd. Second end 112 of capacitor 110 is connected to gate 241 of fourth transistor Q4 240 and drain 233 of third transistor Q3 230. Gate 211 of first transistor Q2 210, gate 221 of second transistor Q2 220, and gate 251 of fifth transistor Q5 250 are tied to row line -ROW 152. Gate 231 of third transistor Q3 230 is tied to drain 213 of first transistor Q1 210. Source 212 of first transistor Q1 210 is tied to column strobe line -STR 168. Source 222 of second transistor Q2 220 is tied to column line DATA 169. Source 232 of third transistor Q3 230 is connected to drain 223 of second transistor Q2 220. Drain 243 of fourth transistor Q4 240 is connected to drain 253 of fifth transistor Q5 250. Source 252 of fifth transistor Q5 250 is connected to anode 101 of pixel Px1 100. Cathode 102 of pixel Px1 100 is connected to negative voltage. Third transistor Q3 230 and fourth transistor Q4 240 are preferably P-FETs. Fifth transistor Q5 250 is preferably an N-FET.

Circuit 50 of Fig. 7 operates as follows: RAMP 190 voltage is raised from 0V to +5V linearly; then dropped to 0V and the cycle is repeated. With capacitor C1 110 discharged, gate 241 of fourth transistor Q4 240 is held at +5V and Q4 240 remains off throughout the ramp cycle. The pixel current is zero. With capacitor C1 110 fully charged (+5V), gate 241 of Q4 240

is held at 0V and Q4 240 turns on as soon as the ramp voltage exceeds about 0.5V (the threshold voltage of Q4 240) and remains on for the rest of the ramp period. The duration of the "on" condition of device Q4 240 during the ramp cycle thus depends upon the analog input voltage stored on capacitor C1 110. With design optimization, this version of the pixel cell may give better gray scale resolution. Circuit 50 of Fig. 7 may, however, have extra power dissipation in the ramp generator.

While this invention has been described in conjunction with specific embodiments thereof, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, the preferred embodiments of the invention as set forth herein are intended to be illustrative, not limiting.



**What is claimed is:**

1. A pixel driver circuit for a video display device having a plurality of pixels arranged in a matrix and using constant amplitude pulses to control the device drive signals, said driver circuit comprising:

5' means for supplying digital pixel brightness input data;  
means for subdividing said digital input data, connected to said supplying means;  
means for converting said subdivided digital input data to analog input data, connected to said subdividing means;  
means for applying said analog input data to said driver circuit, connected to said  
10 converting means;  
at least one capacitor connected to said applying means; and  
means for feeding said analog input data to one of said plurality of pixels, connected to said applying means and to said at least one capacitor.

2. The driver circuit of claim 1, wherein said applying means comprises at least one p-type field effect transistor.

3. The driver circuit of claim 1, wherein said means for feeding said analog input data to one of said plurality of pixels comprises at least one p-type field effect transistor.

4. The driver circuit of claim 1, wherein said digital input data comprise 8 bits of data.

5. The driver circuit of claim 1, wherein said subdivided digital input data comprise a first half-byte of four higher order bits and a second half-byte of four lower order bits.

6. The driver circuit of claim 5, wherein said converting means comprises a first digital-to-analog converter for said four higher order bits and a second digital-to-analog converter for said four lower order bits.

7. The driver circuit of claim 6, wherein said first digital-to-analog converter converts said four higher order bits of digital input data into analog data of a first plurality of current values.

8. The driver circuit of claim 7, wherein said first plurality of current values comprises 16 discrete steps of 16nA each, to cover a range of 0 to 256nA.

9. The driver circuit of claim 6, wherein said second digital-to-analog converter converts said four lower order bits of digital input data into analog data of a second plurality of current values.

10. The driver circuit of claim 9, wherein said second plurality of current values comprises 16 discrete steps of 1nA each, to cover a range of 0 to 16nA.

11. The driver circuit of claim 1, wherein said applying means comprises at least one p-type field effect transistor and at least one n-type field effect transistor.

12. A pixel driver circuit for a video display device having a plurality of pixels arranged in a matrix and using constant amplitude pulses to control the device drive signals, said driver circuit comprising:

means for supplying digital pixel brightness input data;

5 means for converting said digital input data to analog input data, connected to said supplying means;

means for applying said analog input data to said driver circuit, connected to said converting means;

at least one capacitor connected to said applying means; and

10 means for feeding said analog input data to one of said plurality of pixels, connected to said applying means and to said at least one capacitor.

13. The driver circuit of claim 12, wherein said applying means comprises at least one p-type field effect transistor.

14. The driver circuit of claim 12, wherein said means for feeding said analog input data to one of said plurality of pixels comprises at least one n-type field effect transistor.

15. The driver circuit of claim 12, wherein said digital input data comprise 8 bits of data.

16. The driver circuit of claim 12, further comprising a strobe column line.

17. The driver circuit of claim 12, further comprising a ramp control line.

18. A method of driving a pixel circuit in a video display device having a plurality of pixels arranged in a matrix and using constant amplitude pulses to control the device drive signals, said method comprising the steps of:

receiving a byte of digital pixel brightness input data;

5 dividing said digital byte into a first half-byte of four higher order bits and a second half-byte of four lower order bits;

converting said first half-byte into a first analog input signal;

converting said second half-byte into a second analog input signal;

applying said first analog input signal and said second analog input signal to said driver circuit;

storing a charge on at least one capacitor in response to said analog input signals;

feeding said first analog input signal and said second analog input signal to one of said plurality of pixels; and

controlling the voltages developed across said at least one capacitor to directly control the total current fed to one of said plurality of pixels.

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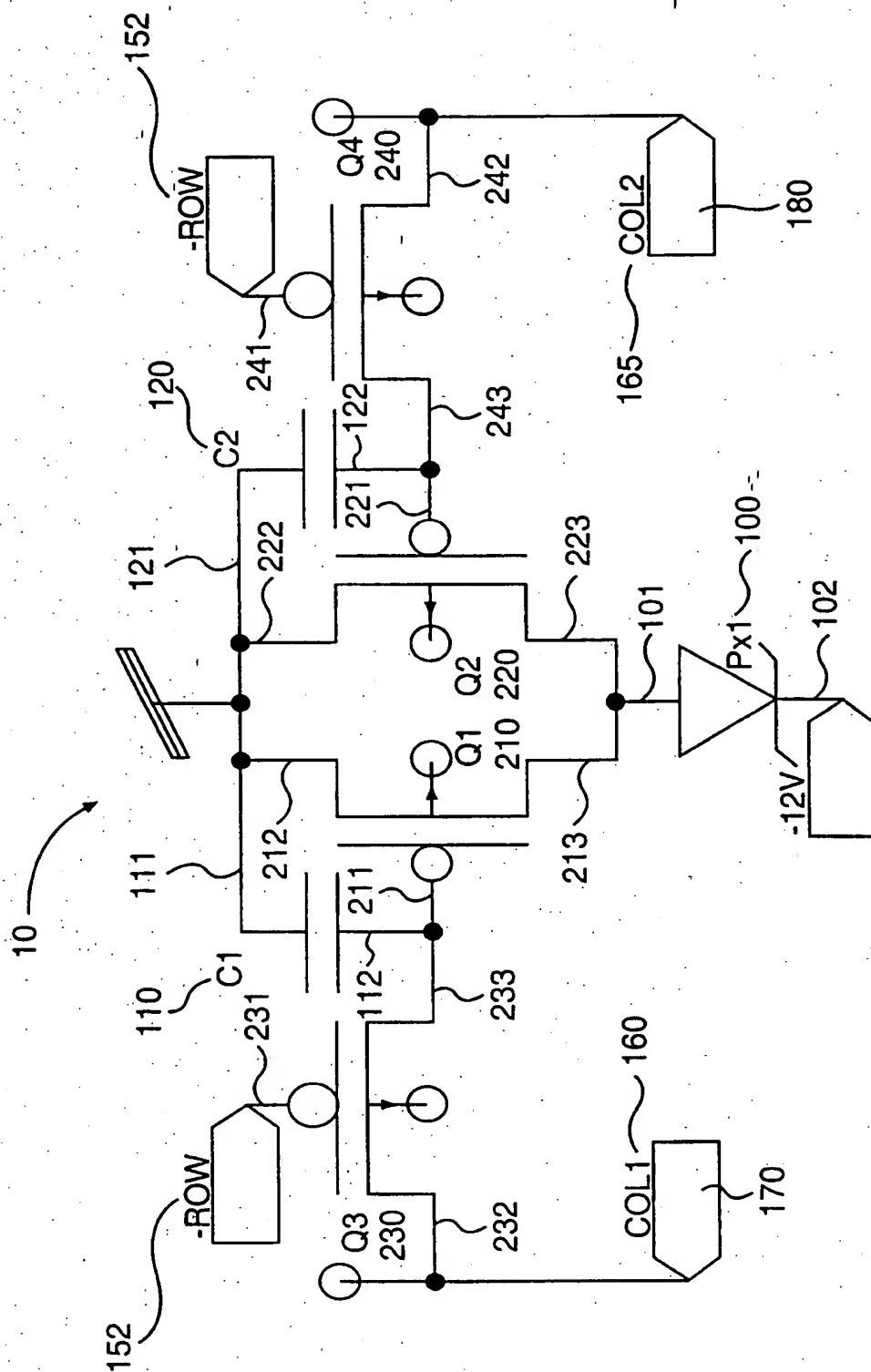
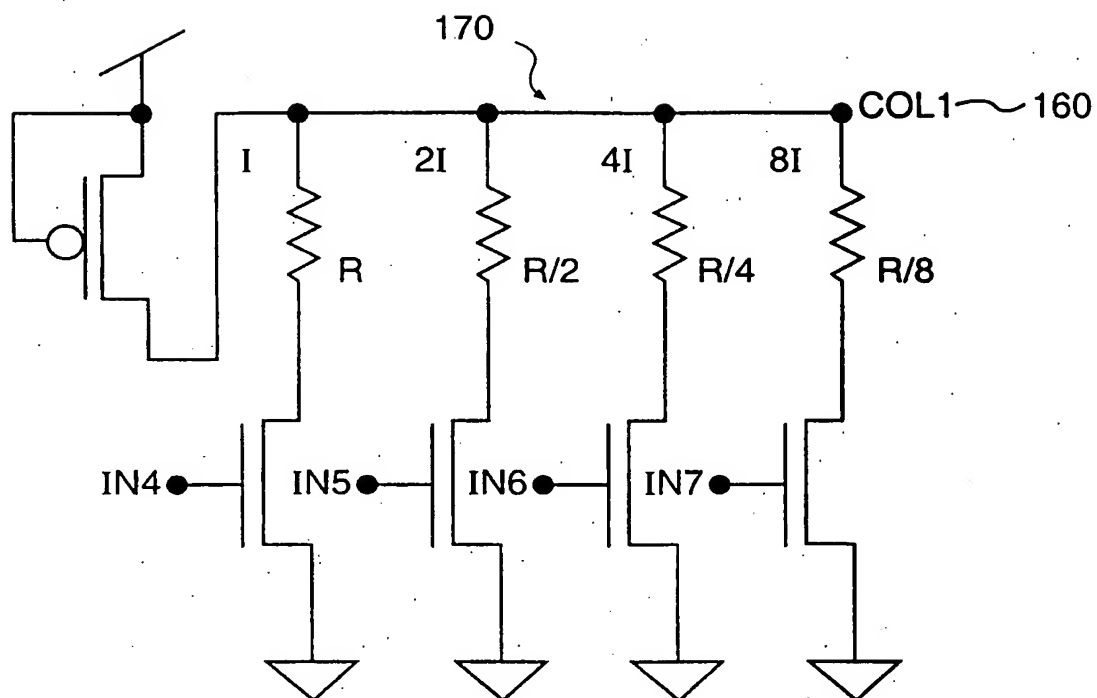
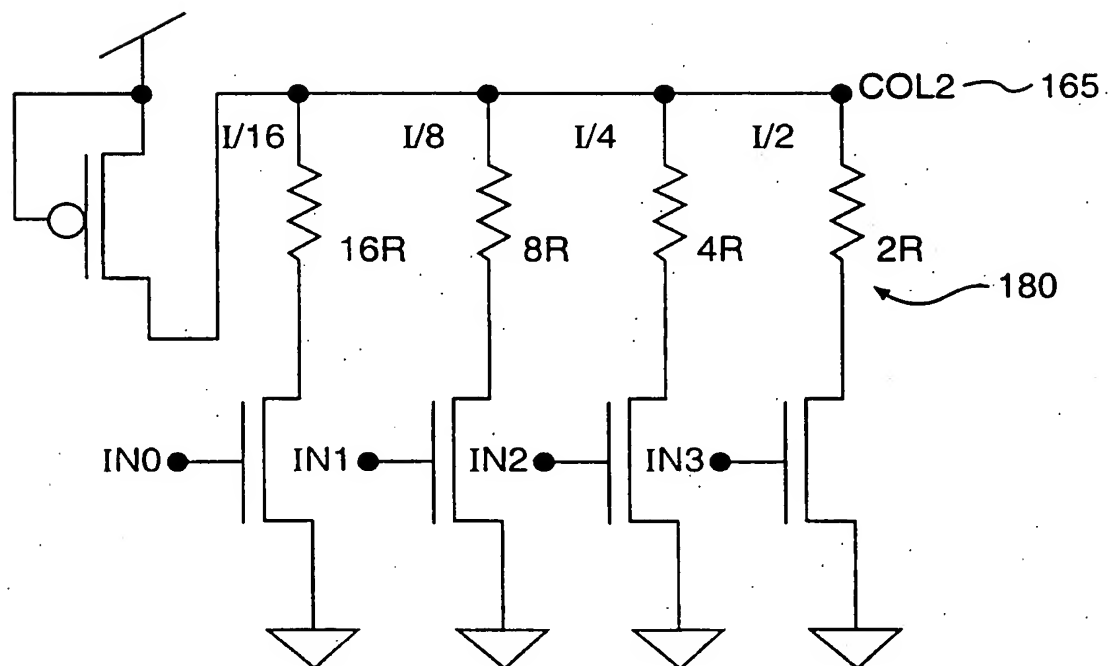


FIG. 1

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**FIG. 2****FIG. 3**

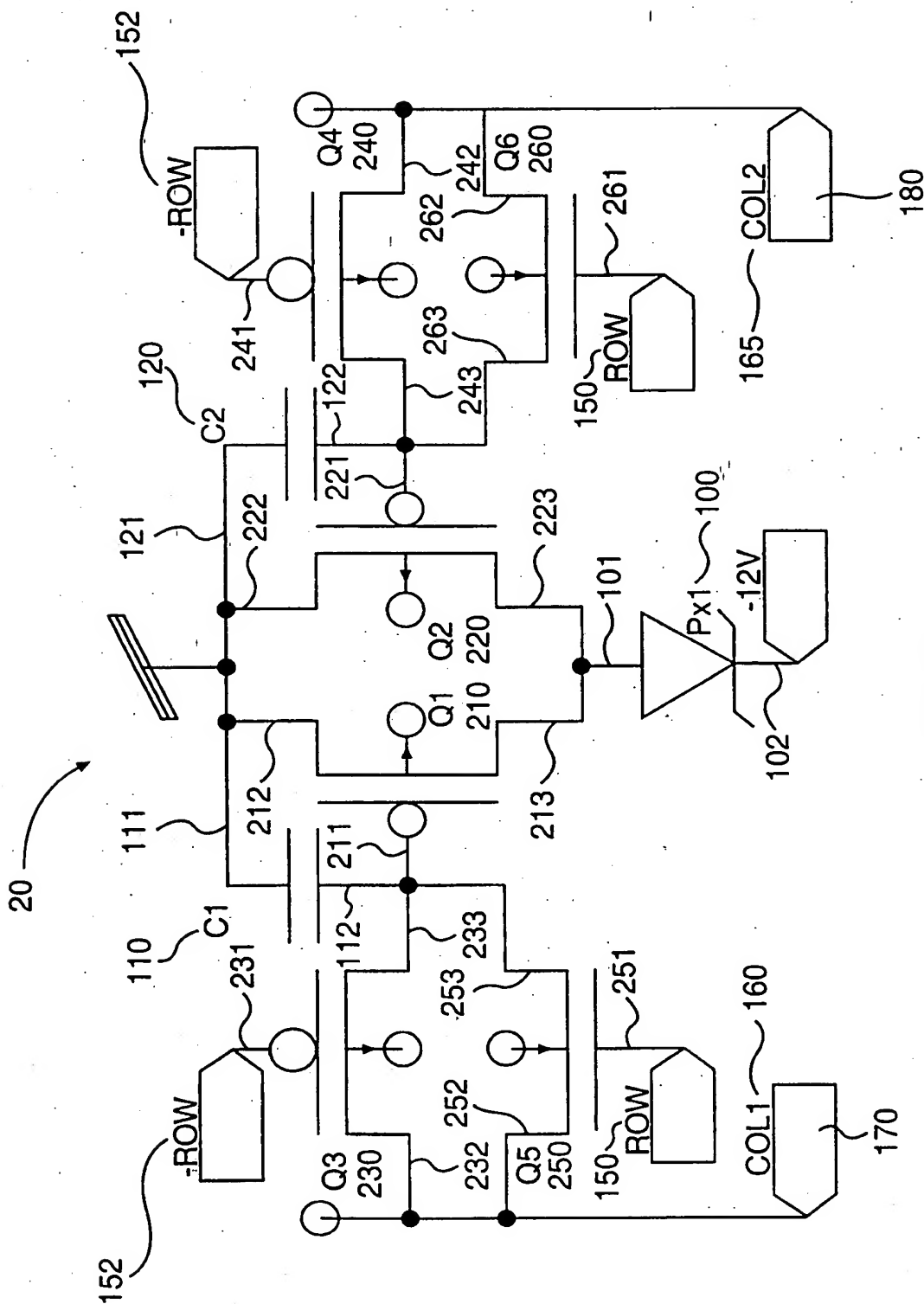


FIG. 4

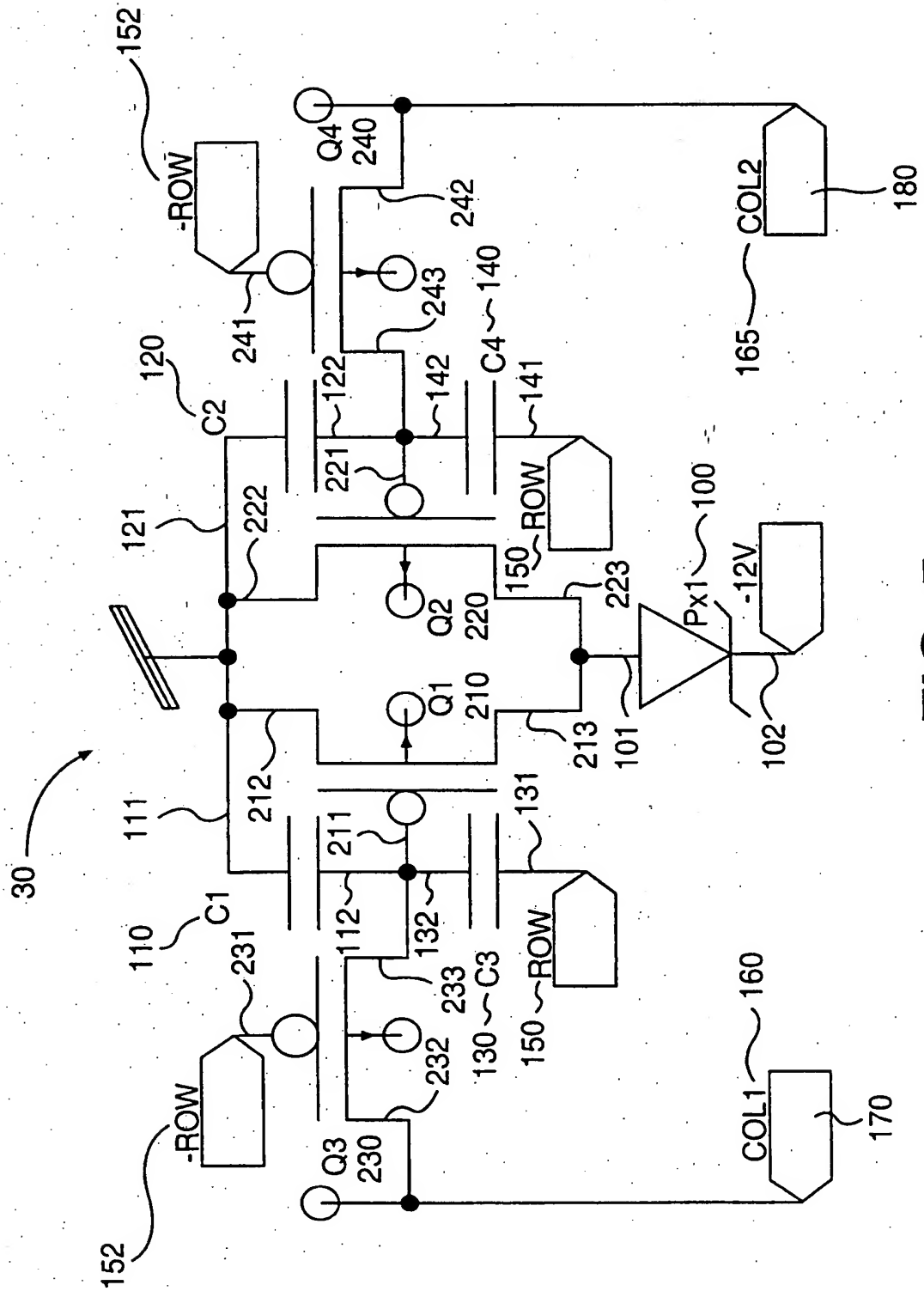
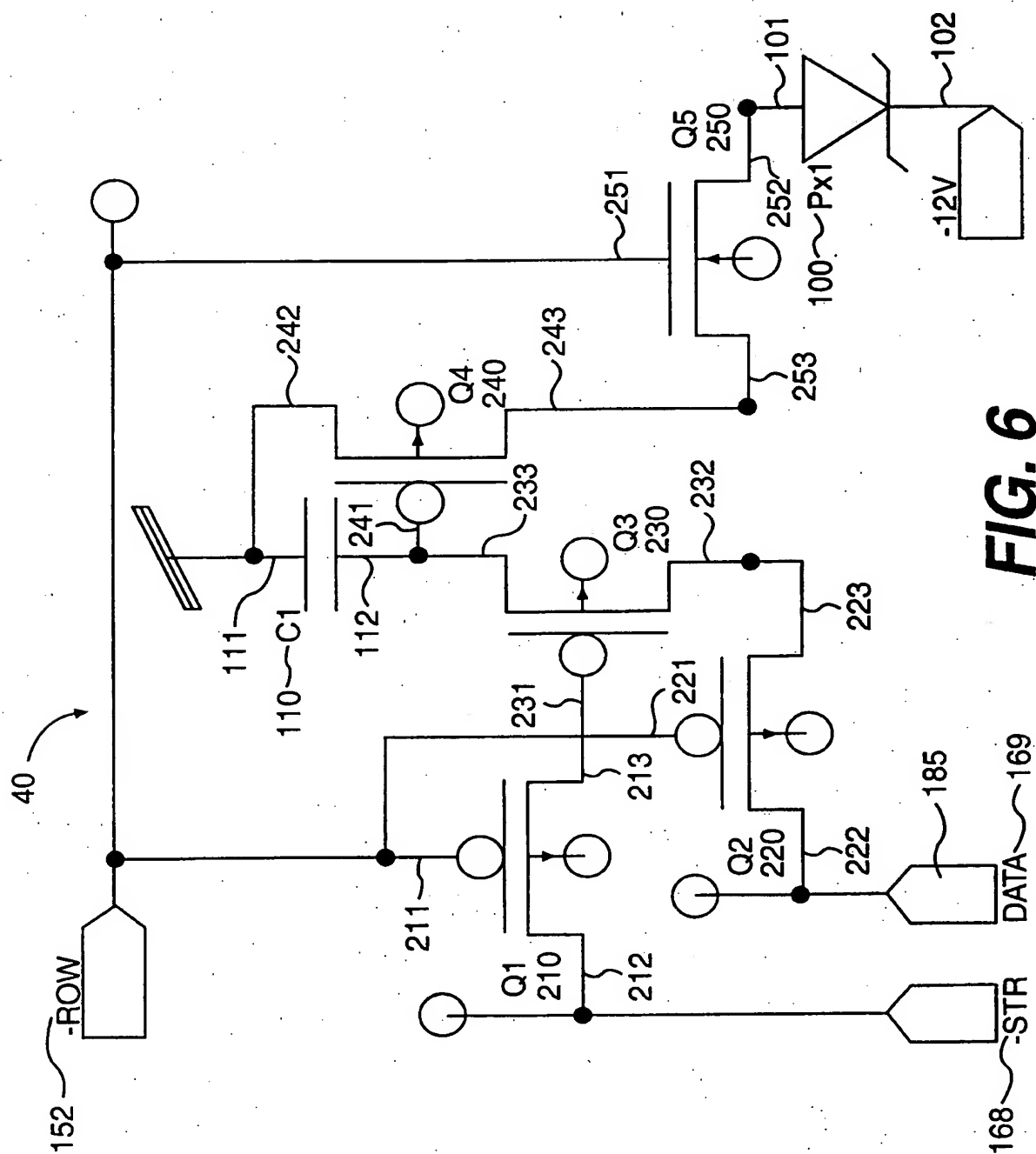
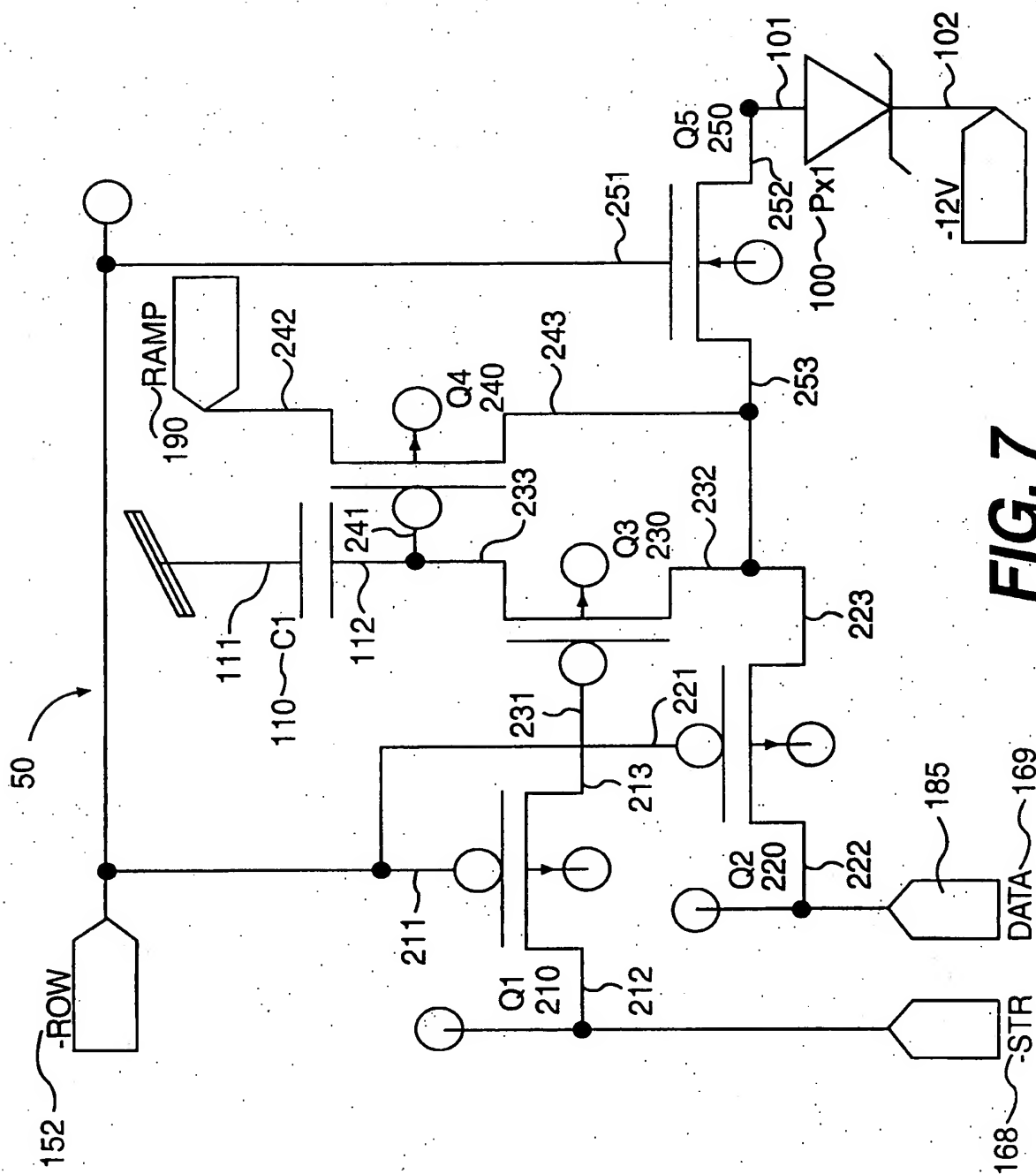


FIG. 5







**FIG. 7**

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US99/07207

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : G09G 3/32; G09G 3/10

US CL : 345/74, 77; 315/169.3

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 345/74, 76-77, 87, 89, 100, 147, 516; 315/169.1, 169.3, 169.4

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,477,110 A (SMITH et al) 19 December 1995, col. 2, lines 13-29 and col. 6, lines 3-25.	1-18
Y	US 5,617,111 A (SAITOH) 01 April 1997, col. 4, lines 51-64 and col. 5, lines 40-54.	1-18
A	US 5,642,017 A (HUSH) 24 June 1997, see figure 2, col. 4, lines 41-64.	1-18



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

07 JULY 1999

Date of mailing of the international search report

17 AUG 1999

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专利申请号: 031061559	申请日: 2003 年 2 月 19 日	<input checked="" type="checkbox"/> 首次检索			
权利要求数目: 12	说明书页数: 5+5	<input type="checkbox"/> 补充检索			
审查员确定的 IPC 分类号: G09G 5/00, G09G 5/10, G09G 3/36					
审查员实际检索的 IPC 分类号: G09G 5/00, G09G 5/10, G09G 5/+, G09G 3/+, G02F1/+, G09F9/+, H04N5/+, G01J3/+, G06T5/+					
机检数据 (数据库名称, 检索要素如关键词等): CNPAT, CNKI, 汤姆森, 汤姆森, 高通#, 沈波#, 液晶, LCD, 像素, 象素, 依赖, 串扰, 高, 低, 阿, 双, 2, 第一, 第二, 亮度, 灰度, 辉度, 延迟#, 闪烁, 闪屏 WPI, EPODOC, PAJ LOW, PASS, HIGH, FILT???, REJECT???, LCD, LIQUID, CRYSTAL, D- ISPLAY, PDXEL?, SPARKL???, FLICK+, CORUSCAT+, GLINT+, RADIANC+, WINK+, inter d dependen???, cross d talk???, reliable, relian???					
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A	US5247169A	1993-09-21	G01J 3/50	全文	1-12
A	US4523230A	1985-06-11	H04N 5/14	全文	1-12
A	CN1207845				1-12





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审查员 (5343)  
2007 年 5 月 27 日

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